

## CLAIMS

1           1. A method of making a charge-coupled device comprising:  
2                   forming an electrically conducting charge transfer channel in a  
3                   semiconductor substrate;  
4                   forming an electrically insulating layer on a surface of the  
5                   substrate;  
6                   forming a layer of gate electrode material on the insulating  
7                   layer;  
8                   forming on the gate material layer a first patterned masking  
9                   layer having apertures that expose regions of the underlying gate material  
10                   layer that are to form gate electrodes;  
11                   electrically doping the first-pattern-exposed regions of the gate  
12                   material layer;  
13                   forming on the gate material layer a second patterned masking  
14                   layer having apertures that expose regions of the underlying gate material  
15                   layer that are to form gaps between gate electrodes; and  
16                   etching the second-pattern-exposed regions of the gate material  
17                   layer.

1           2. The method of claim 1 further comprising removal of the first  
2                   patterned masking layer after electrically doping first-pattern-exposed  
3                   regions of the gate material layer.

1           3. The method of claim 1 further comprising removal of the second  
2                   patterned masking layer after etching second-pattern-exposed regions of the  
3                   gate material layer.

1           4. The method of claim 1 wherein the first-pattern-exposed regions  
2 of the gate material layer are electrically doped before the second-pattern-  
3 exposed regions of the gate material layer are etched.

1           5. The method of claim 1 wherein electrically doping first-pattern-  
2 exposed regions of the gate material layer comprises ion implantation of a  
3 selected electrical dopant into the first-pattern-exposed regions of the gate  
4 material layer.

1           6. The method of claim 1 wherein etching the second-pattern-  
2 exposed regions of the gate material layer comprises plasma etching the  
3 second-pattern-exposed regions of the gate material layer.

1           7. The method of claim 1 further comprising heat treating the  
2 electrically-doped and etched gate electrode material layer to diffuse the  
3 electrical dopant through the gate material layer thickness.

1           8. The method of claim 7 wherein heat treating the electrically-  
2 doped and etched gate electrode material layer comprises annealing the gate  
3 material layer.

1           9. The method of claim 7 wherein heat treating the electrically-  
2 doped and etched gate electrode material layer comprises oxidation of the  
3 gate material layer.

1           10. The method of claim 7 wherein forming a first patterned  
2 masking layer and forming a second patterned masking layer each comprise  
3 forming a masking layer having a pattern the apertures of which are

4 characterized by an extent accounting for lateral dopant diffusion during the  
5 heat treatment.

1           11. The method of claim 1 wherein forming an electrically  
2 conducting charge transfer channel in a semiconductor substrate comprises  
3 ion implantation of a selected electrical dopant into a silicon substrate, the  
4 selected electrical dopant being of a conductivity type opposite that of the  
5 silicon substrate.

1           12. The method of claim 1 wherein forming an electrically  
2 insulating layer on a surface of the substrate comprises forming a layer of  
3 oxide on the substrate surface.

1           13. The method of claim 1 wherein forming a layer of gate electrode  
2 material on the insulating layer comprises depositing a layer of amorphous  
3 silicon on the insulating layer.

1           14. The method of claim 1 wherein forming a layer of gate electrode  
2 material on the insulating layer comprises depositing a layer of polysilicon on  
3 the insulating layer.

1           15. The method of claim 1 wherein forming a first patterned  
2 masking layer and forming a second patterned masking layer each comprise  
3 forming a layer of photoresist that is photolithographically patterned.

1           16. The method of claim 1 further comprising:

2 forming a third patterned masking layer on the gate material layer,  
3 the third patterned masking layer having apertures that expose regions of  
4 the gate material layer;

5 depositing a metal layer that contacts the third-pattern-exposed  
6 regions of the gate material layer; and

7 siliciding the gate material layer by heat treating the metal and gate  
8 material layers.

1 17. The method of claim 1 further comprising:

2 forming an electrically insulating electrode separation layer on  
3 the electrically doped and etched gate electrode material layer;

4 forming an upper gate electrode material layer on the insulating  
5 electrode separation layer;

6 forming on the upper gate material layer a third patterned  
7 masking layer having apertures that expose regions of the underlying upper  
8 gate material layer that are to form gate electrodes;

9 electrically doping the third-pattern-exposed regions of the  
10 upper gate material layer;

11 forming on the upper gate material layer a fourth patterned  
12 masking layer having apertures that expose regions of the underlying upper  
13 gate material layer that are to form gaps between gate electrodes; and

14 etching the fourth-pattern-exposed regions of the upper gate  
15 material layer.

1 18. A method of making a charge-coupled device comprising:

2 forming an electrically conducting charge transfer channel in a  
3 semiconductor substrate;

4 forming on a substrate surface a first patterned masking layer  
5 having apertures that expose regions of the underlying substrate surface that  
6 are to form gate electrodes;  
7 electrically doping the first-pattern-exposed regions of the  
8 substrate surface;  
9 forming on the substrate surface a second patterned masking  
10 layer having apertures that expose regions of the underlying substrate  
11 surface layer that are to form gaps between gate electrodes; and  
12 etching the second-pattern-exposed regions of the substrate  
13 surface.

1 19. A method of making electrically conducting electrodes

2 comprising:

3 forming an electrically insulating layer on a surface of a

4 substrate;

5 forming a layer of electrode material on the insulating layer;

6 forming on the electrode material layer a first patterned

7 masking layer having apertures that expose regions of the underlying

8 electrode material layer that are to form electrodes;

9 electrically doping the first-patterned-exposed regions of the

10 electrode material layer;

11 forming on the electrode material layer a second patterned

12 masking layer having apertures that expose regions of the underlying

13 electrode material layer that are to form gaps between electrodes; and

14 etching the second-patterned-exposed regions of the electrode

15 material layer.

1                   20     A method of making electrically conducting electrodes  
2     comprising:  
3                   forming on a substrate surface a first patterned masking layer  
4     having apertures that expose regions of the underlying substrate surface that  
5     are to form electrodes;  
6                   electrically doping the first-pattern-exposed regions of the  
7     substrate surface;  
8                   forming on the substrate surface a second patterned masking  
9     layer having apertures that expose regions of the underlying substrate  
10    surface layer that are to form gaps between electrodes; and  
11                  etching the second-pattern-exposed regions of the substrate  
12    surface.